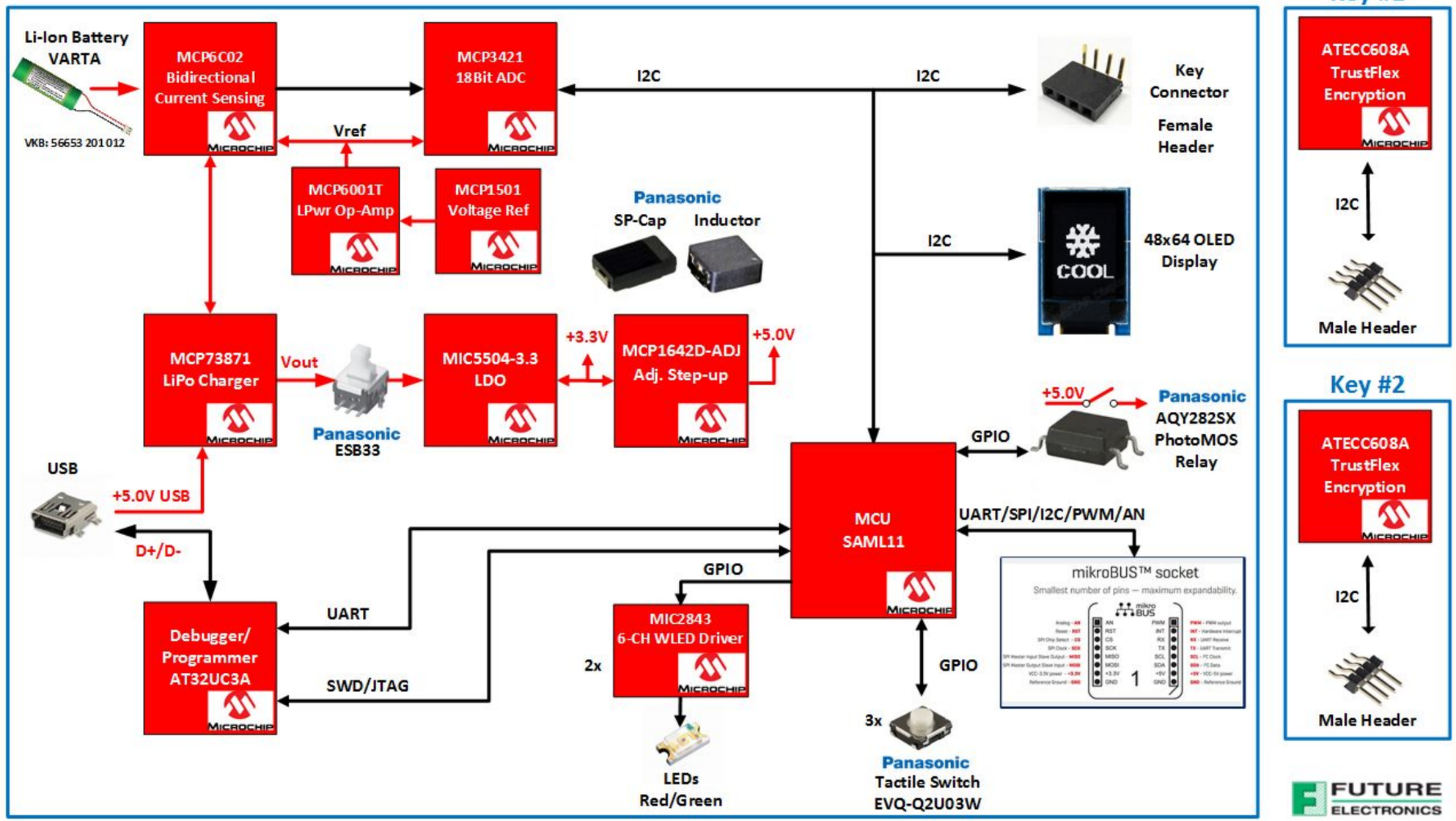
GoodLock rev 1.1



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Designed by: C. Zhao	Drawn by: C. Zhao
Checked by: H. Letourneau	Approved by: M. Bernier

Future Electronics - System Design Center NA
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

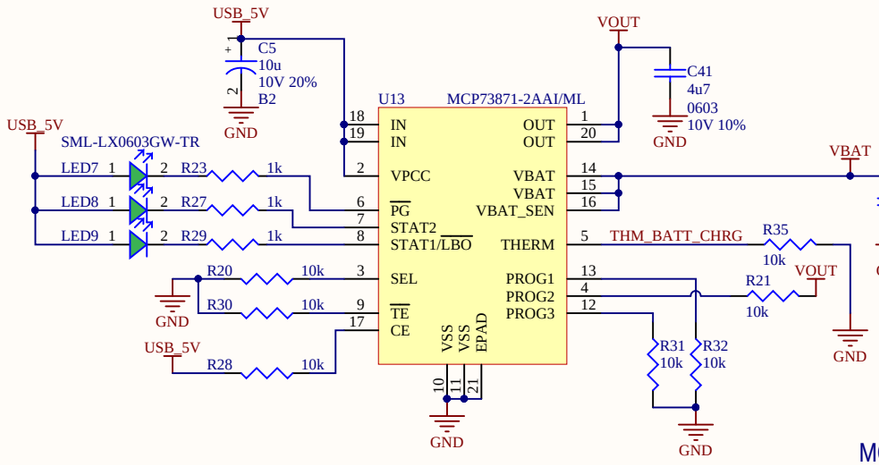
Project Name: GoodLock Rev 1.1

Title: Block Diagram

Size: B | Dwg No.: FEN-501044-SCH-R1.1 | Rev: 1.1

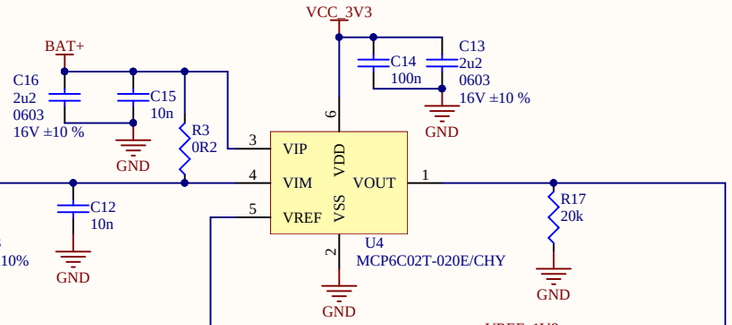
Date: 2/20/2020 | Sheet: 1 of 5 | Variant: [No Variations]

MCP73871 Battery Charger

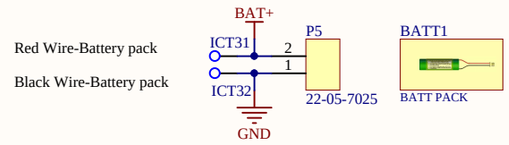


Charge current is set to 100mA

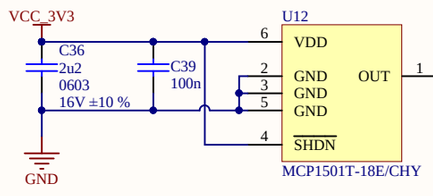
MCP6C02T Current Sensing



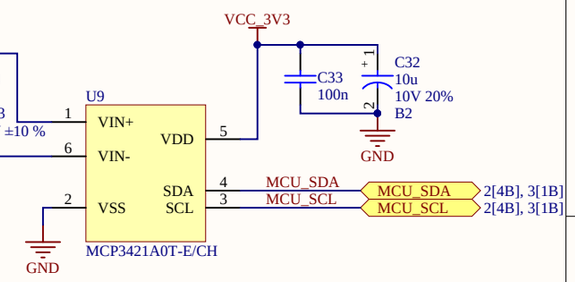
3.65V Battery Pack(Cell)



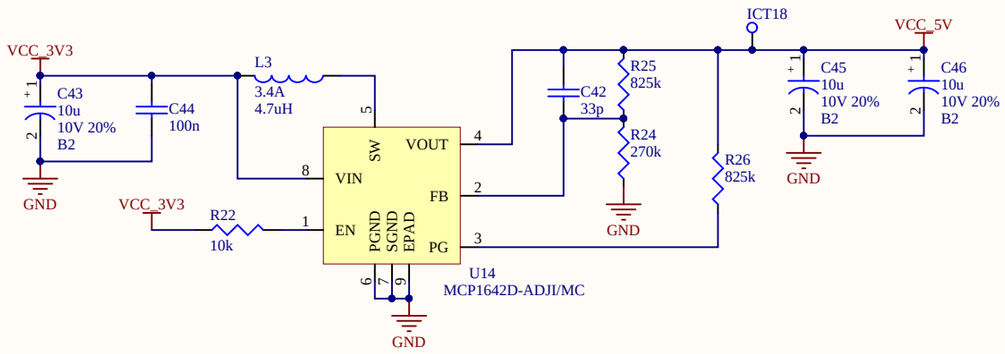
MCP1501T H-Precision Voltage Reference



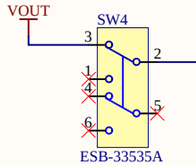
MCP3421 18-bit ADC



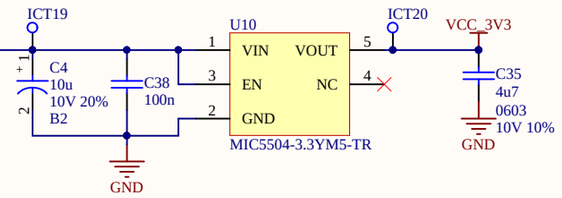
MCP1642D Boost Regulator



Power Switch



MIC5504 LDO



All capacitors and resistors are in 0402 package otherwise indicated.

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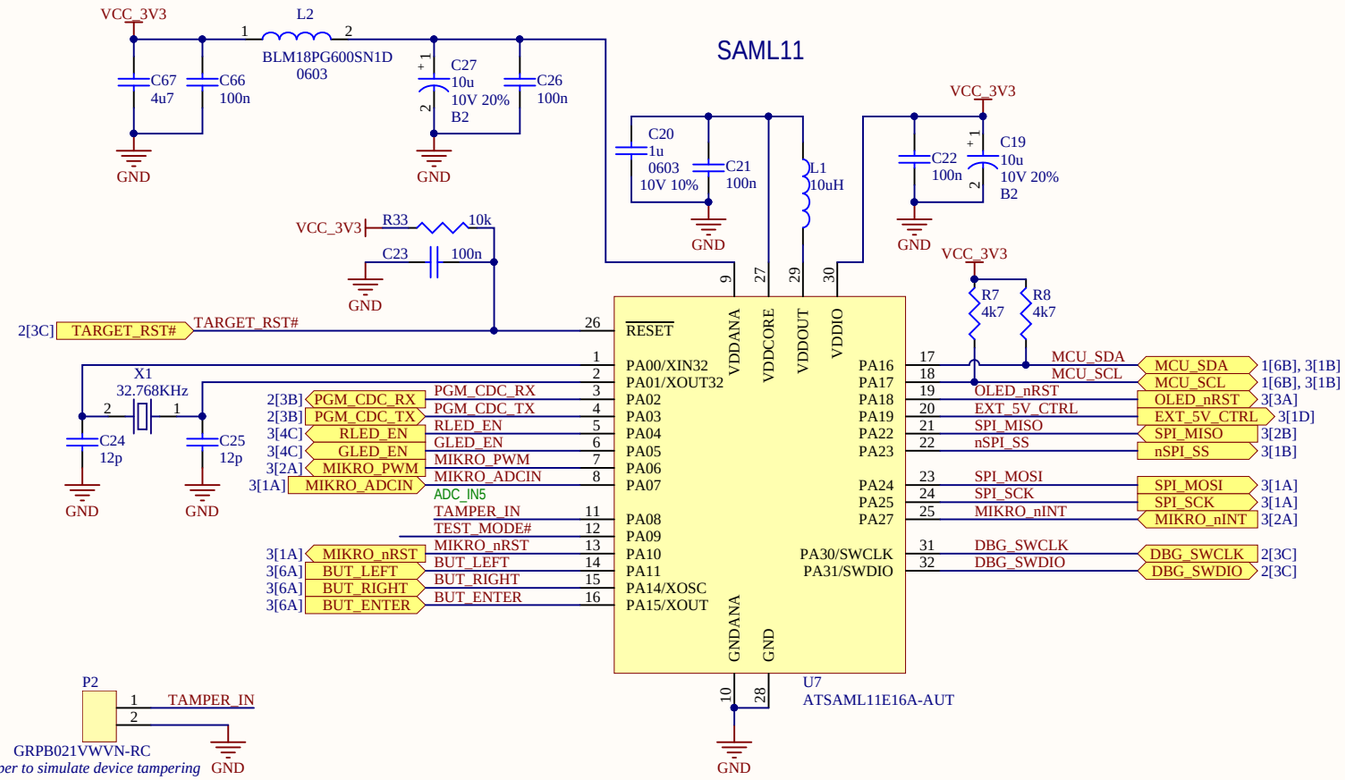
Pointe-Claire, Quebec, Canada
H9R 5C7

Project Name	GoodLock Rev 1.1
Title	Power
Designed by	C. Zhao
Drawn by	C. Zhao
Checked by	H. Letourneau
Approved by	M. Bernier
Size	B
Dwg No.	FEN-501044-SCH-R1.1
Rev	1.1
Date	2/20/2020
Sheet	2 of 5
Variant:	[No Variations]



Assembly

Fiducial Fiducial Fiducial Fiducial Fiducial

Fiducial Fiducial Fiducial Fiducial Fiducial

Tape1

Double side tape 10 x 10mm

All capacitors and resistors are in 0402 package otherwise indicated.

Designed by	C. Zhao
Drawn by	C. Zhao
Checked by	H. Letourneau
Approved by	M. Bernier

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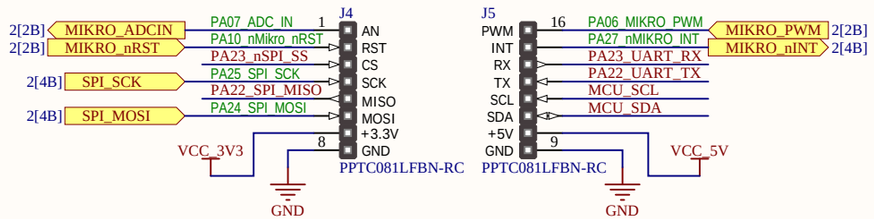
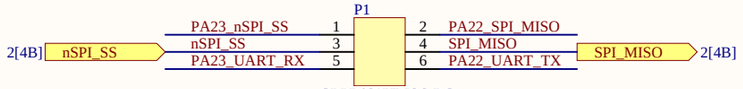
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

Project Name	GoodLock Rev 1.1
Title	MCU
Size	B
Dwg No.	FEN-501044-SCH-R1.1
Rev	1.1
Date	2/20/2020
Sheet	3 of 5
Variant:	[No Variations]

MikroBus Header

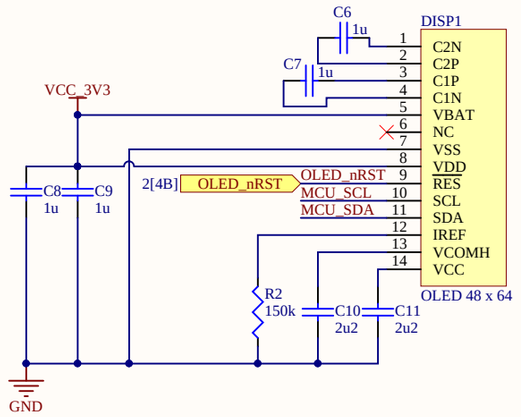
IO Voltage range on MIKROBUS is 0-3.3V



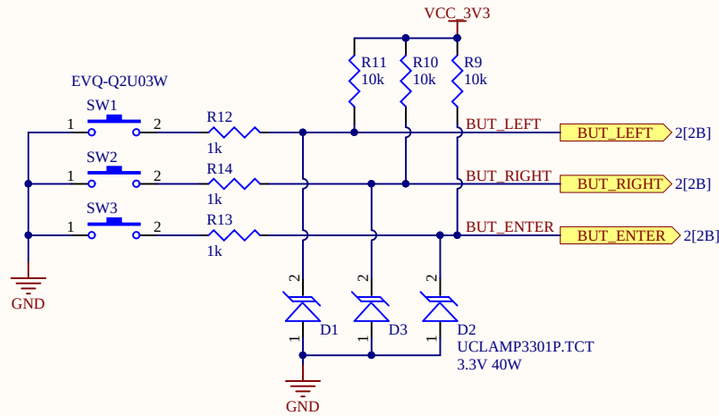


Place Jumper on P1 1-3 and 2-4 for SPI operation
Place Jumper on P1 3-5 and 4-6 for UART operation

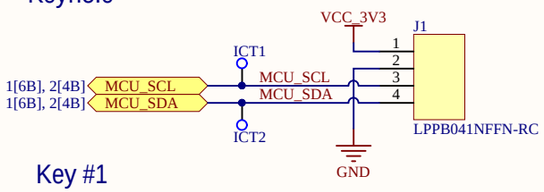
OLED LCD 48 x 64



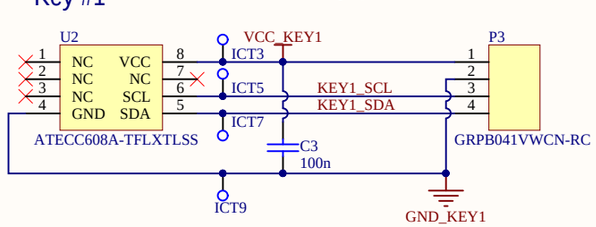
Buttons



Keyhole



Key #1



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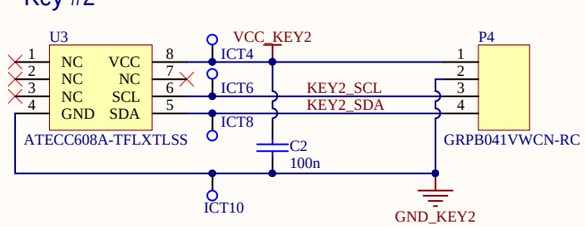
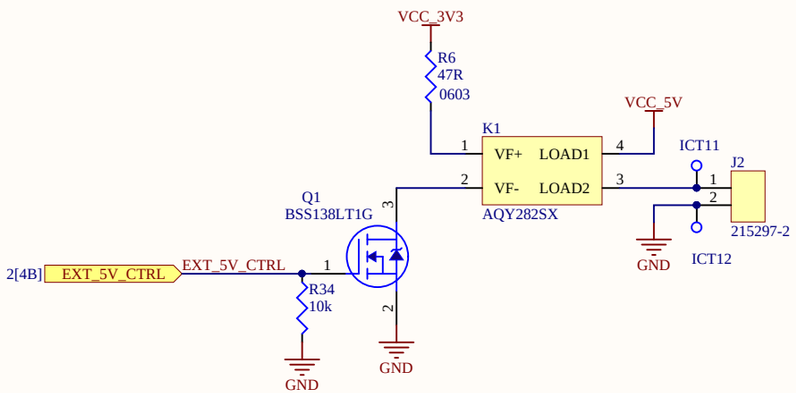
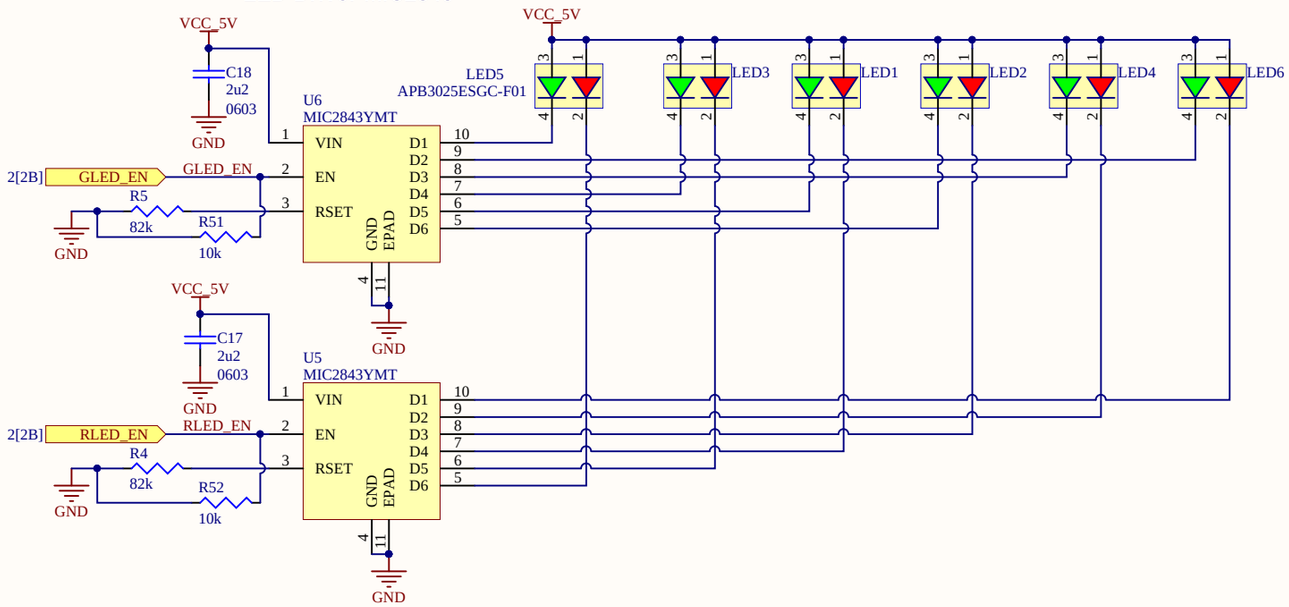


5V DC Ouput (max 0.5A)



LED Driver MIC2843



All capacitors and resistors are in 0402 package otherwise indicated.

FUTURE ELECTRONICS

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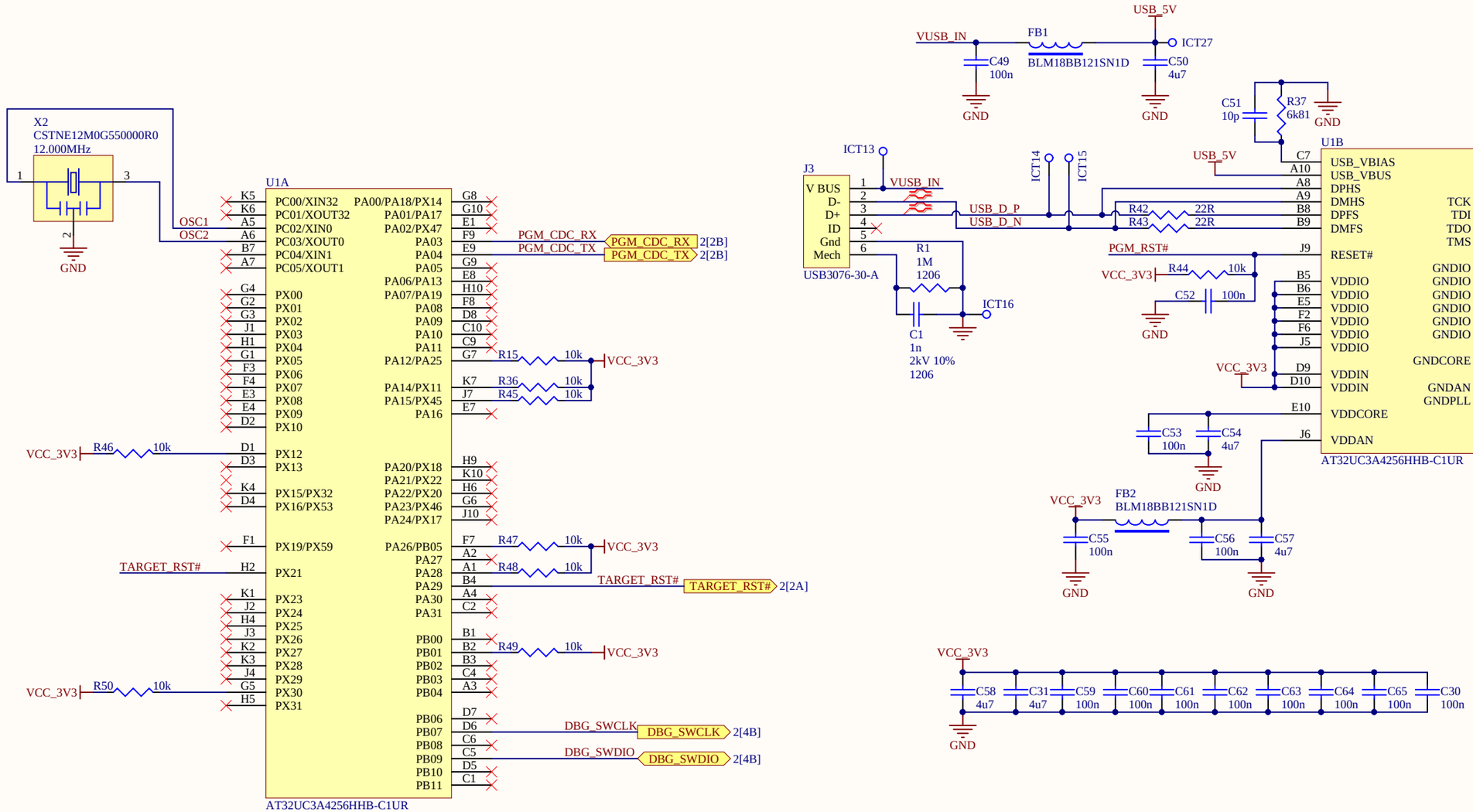
Pointe-Claire, Quebec, Canada
H9R 5C7

Project Name	GoodLock Rev 1.1
Title	Peripherals
Designed by	C. Zhao
Drawn by	C. Zhao
Checked by	H. Letourneau
Approved by	M. Bernier
Size	B
Dwg No.	FEN-501044-SCH-R1.1
Rev	1.1
Date	2/20/2020
Sheet	4 of 5
Variant:	[No Variations]

DEBUGGER/PROGRAMMER



All capacitors and resistors are in 0402 package otherwise indicated.

FUTURE ELECTRONICS

AEG Engineering Tomorrow's Ideas

Future Electronics - System Design Center NA
237 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

Designed by	C. Zhao
Drawn by	C. Zhao
Checked by	H. Letourneau
Approved by	M. Bernier

Project Name: GoodLock Rev 1.1

Title: MCU

Size: B | Dwg No. FEN-501044-SCH-R1.1 | Rev 1.1

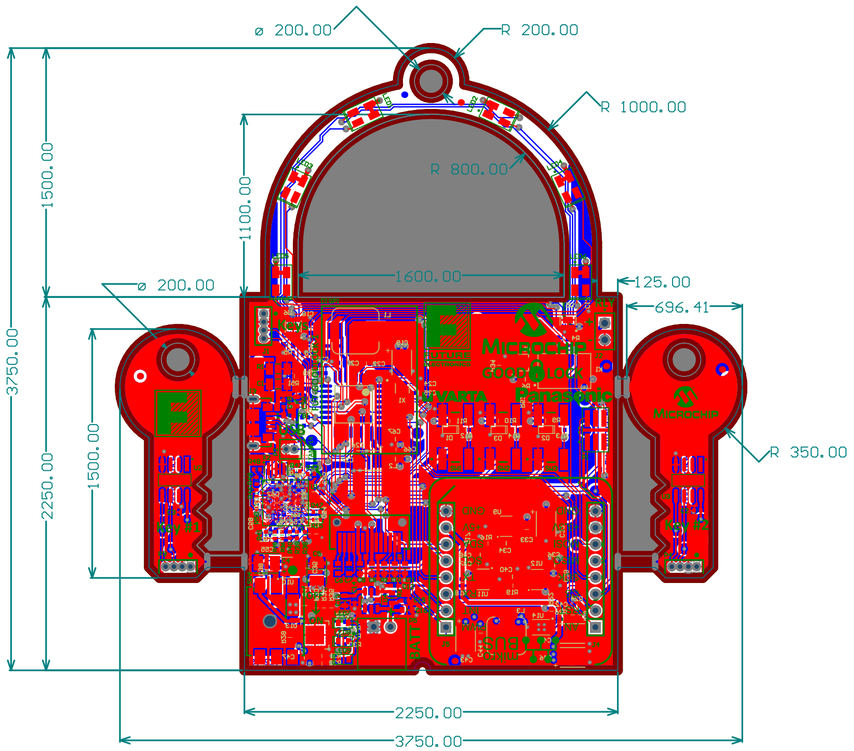
Date 2/20/2020 | Sheet 5 of 5 | Variant: [No Variations]

Layers	Top Layer	Bottom Layer	PWR	GND		

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	NA	6 mil	8 mil	NA	NA
Bottom Layer	NA	6 mil	8 mil	NA	NA

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.2	
5	PWR	Copper	1.40mil		
6	Dielectric2	FR-4 HTg	48.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 HTg	3.80mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg ☒ Metal Core ☐ Other ☐ _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz ☒ 0.75oz ☐ 1oz ☐ Other ☐ _____

5. FINISH - HASL RoHS ☐ HASL ☐ Immersion Silver ☐ Immersion Tin ☐ ENIG ☒
   Other ☐ _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN ☐ WHITE ☐ BLUE ☐ Other ☒ RED

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM ☒ TOP ONLY ☐ BOTTOM ONLY ☐ NONE ☐
   - WHITE ☒ BLACK ☐ Other ☐ _____

8. IMPEDANCE CONTROL - NO ☐ YES ☒ SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
    - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

☑

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Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

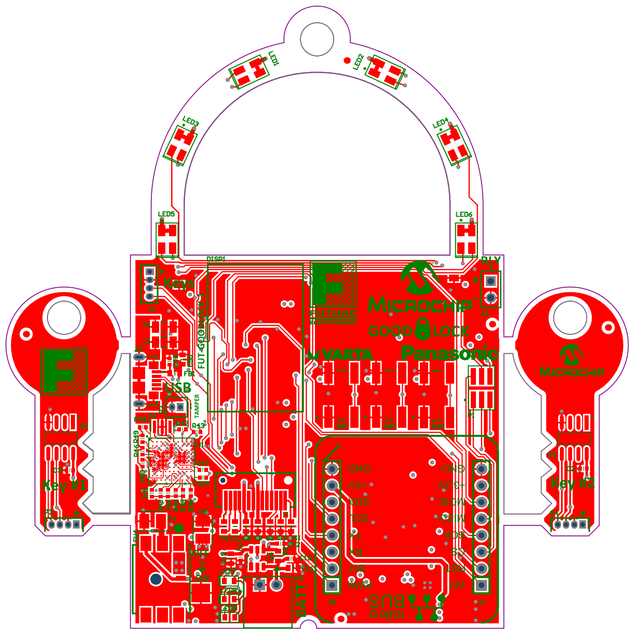
Designed by: C. Zhao	Drawn by: C. Zhao		
Checked by: H. Letoumeau	Approved by: M. Bernier		
Project #	GoodLock		
Title:	GoodLock		
Size: B	DWG NO: FEN-501044-PCB-R1.1		REV: 1.1
Date: 2/20/2020		Sheet 1 of 1	

Layers	Top Layer					

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	NA	6 mil	8 mil	NA	NA
	NA	6 mil	8 mil	NA	NA

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.2	
5	PWR	Copper	1.40mil		
6	Dielectric2	FR-4 HTg	48.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 HTg	3.80mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg [X] Metal Core [ ] Other [ ] _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz [X] 0.75oz [ ] 1oz [ ] Other [ ] _____

5. FINISH - HASL RoHS [ ] HASL [ ] Immersion Silver [ ] Immersion Tin [ ] ENIG [X]
   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN [ ] WHITE [ ] BLUE [ ] Other [X] RED

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [X] TOP ONLY [ ] BOTTOM ONLY [ ] NONE [ ]
   - WHITE [X] BLACK [ ] Other [ ] _____

8. IMPEDANCE CONTROL - NO [ ] YES [X] SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
    - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

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Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Designed by: C. Zhao	Drawn by: C. Zhao	Project # GoodLock	
Checked by: H. Letoumeau	Approved by: M. Bernier	Title: GoodLock	
		Size: B	DWG NO: FEN-501044-PCB-R1.1 REV: 1.1
		Date: 2/20/2020	Sheet 1 of 1

Layers				GND		

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
	NA	6 mil	8 mil	NA	NA
	NA	6 mil	8 mil	NA	NA

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
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5	PWR	Copper	1.40mil		
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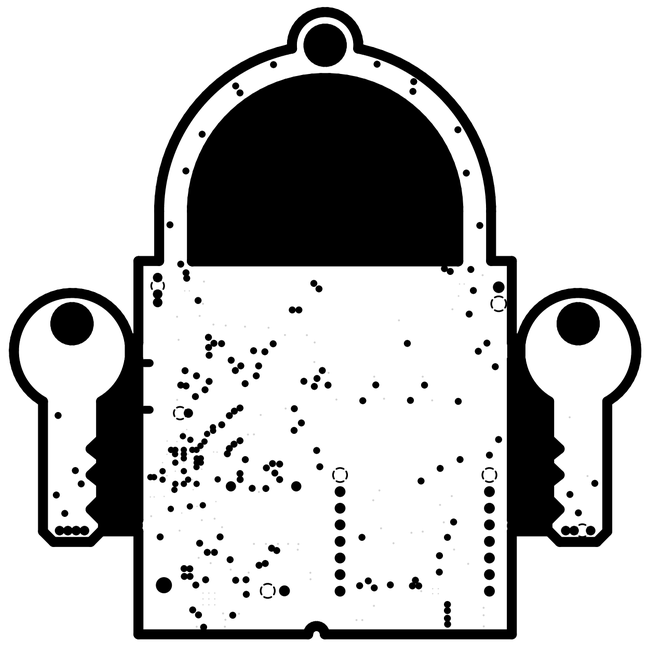
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 HTg	3.80mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg ☒ Metal Core ☐ Other ☐ _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz ☒ 0.75oz ☐ 1oz ☐ Other ☐ _____

5. FINISH - HASL RoHS ☐ HASL ☐ Immersion Silver ☐ Immersion Tin ☐ ENIG ☒
   Other ☐ _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN ☐ WHITE ☐ BLUE ☐ Other ☒ RED

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM ☒ TOP ONLY ☐ BOTTOM ONLY ☐ NONE ☐
   - WHITE ☒ BLACK ☐ Other ☐ _____

8. IMPEDANCE CONTROL - NO ☐ YES ☒ SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
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14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

☑

Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

Designed by: C. Zhao	Drawn by: C. Zhao	Project # GoodLock	
Checked by: H. Letourneau	Approved by: M. Bernier	Title: GoodLock	
		Size: B	DWG NO: FEN-501044-PCB-R1.1 REV: 1.1
		Date: 2/20/2020	Sheet 1 of 1

Layers						
			PWR			

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
	NA	6 mil	8 mil	NA	NA
	NA	6 mil	8 mil	NA	NA

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.2	
5	PWR	Copper	1.40mil		
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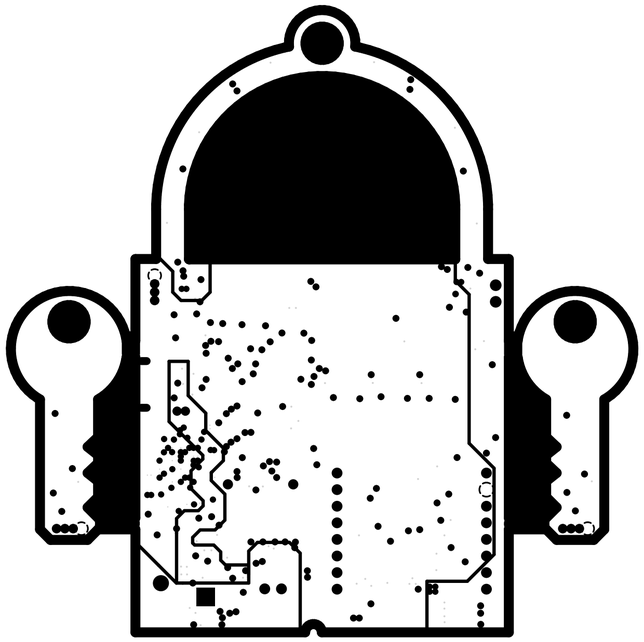
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 HTg	3.80mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg ☒ Metal Core ☐ Other ☐ _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz ☒ 0.75oz ☐ 1oz ☐ Other ☐ _____

5. FINISH - HASL RoHS ☐ HASL ☐ Immersion Silver ☐ Immersion Tin ☐ ENIG ☒
   Other ☐ _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN ☐ WHITE ☐ BLUE ☐ Other ☒ RED

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM ☒ TOP ONLY ☐ BOTTOM ONLY ☐ NONE ☐
   - WHITE ☒ BLACK ☐ Other ☐ _____

8. IMPEDANCE CONTROL - NO ☐ YES ☒ SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
    - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

☑

Future Electronics – System Design Center NA
237 Hymus Blvd
Pointe-Claire, Quebec, Canada
H9R 5C7

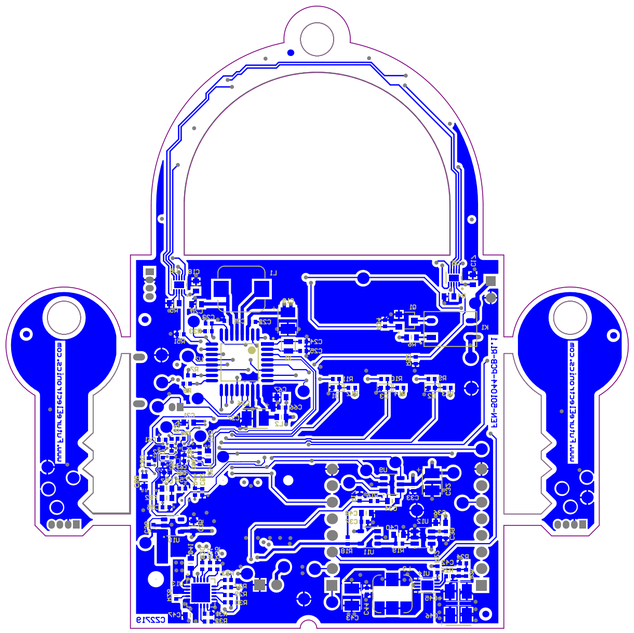
Designed by: C. Zhao	Drawn by: C. Zhao	Project # GoodLock	
Checked by: H. Letourneau	Approved by: M. Bernier	Title: GoodLock	
		Size: B	DWG NO: FEN-501044-PCB-R1.1 REV: 1.1
		Date: 2/20/2020	Sheet 1 of 1

Layers						
		Bottom Layer				

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
	NA	6 mil	8 mil	NA	NA
Bottom Layer	NA	6 mil	8 mil	NA	NA

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 HTg	3.80mil	4.2	
5	PWR	Copper	1.40mil		
6	Dielectric2	FR-4 HTg	48.00mil	4.2	
7	GND	Copper	1.40mil		
8	Dielectric3	FR-4 HTg	3.80mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg ☒ Metal Core ☐ Other ☐ _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz ☒ 0.75oz ☐ 1oz ☐ Other ☐ _____

5. FINISH - HASL RoHS ☐ HASL ☐ Immersion Silver ☐ Immersion Tin ☐ ENIG ☒
   Other ☐ _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN ☐ WHITE ☐ BLUE ☐ Other ☒ RED

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM ☒ TOP ONLY ☐ BOTTOM ONLY ☐ NONE ☐
   - WHITE ☒ BLACK ☐ Other ☐ _____

8. IMPEDANCE CONTROL - NO ☐ YES ☒ SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

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AEG Engineering Tomorrow's Ideas

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